WJEC CBAC

Learning Objectives:

At the end of this topic you will be able to;

- ☑ analyse and design a flash converter based on comparators to meet a given specification;
- ☑ recall the factors affecting the resolution of a flash converter;
- ☑ calculate the resolution of a n-bit flash converter using the formula:

  $$\text{resolution} = \text{input voltage range} / 2^n;$$

- ☑ analyse and design a priority encoder to meet a given specification;

Analogue to Digital Conversion

The process is now the opposite of that studied in Topic 5.2.2. Now we wish to turn an analogue signal into a digital one. To be more precise, we want to develop a system which will output a bigger and bigger binary number as the analogue input voltage grows bigger and bigger.

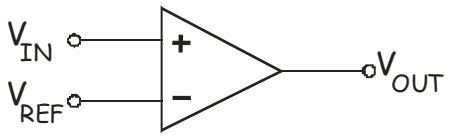
Usually this means outputting a binary number twice as big when the input voltage is twice as big. Suppose that the input voltage changes from V_{IN} to $2V_{IN}$. The digital output then changes from the binary number xxxx to 2(xxxx).

There are a number of ways to design such a circuit. We will base ours on the behaviour of comparators, studied earlier in ET2 section 2.6.1. This type of ADC is known as a **flash converter**.

The content of the following section is a reminder, and is non-examinable!
It is aimed at improving your understanding of the flash converter.

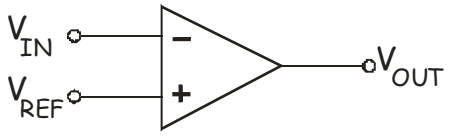
The output of a comparator is always saturated. It is either in positive saturation, as close as possible to the positive supply voltage rail, or in negative saturation, as close as possible to the negative supply voltage rail. The relative size of the two input voltages decides which it is. Usually, one input is provided as a reference voltage, V_{REF}, against which to compare the input voltage V_{IN}.

When the reference voltage is connected to the inverting input:



$V_{OUT} = +V_{SAT}$ when V_{IN} is bigger than V_{REF}.
$V_{OUT} = -V_{SAT}$ when V_{IN} is smaller than V_{REF}.
($+V_{SAT}$ = positive saturation voltage, $-V_{SAT}$ = negative saturation voltage.)

When the reference voltage is connected to the non-inverting input:

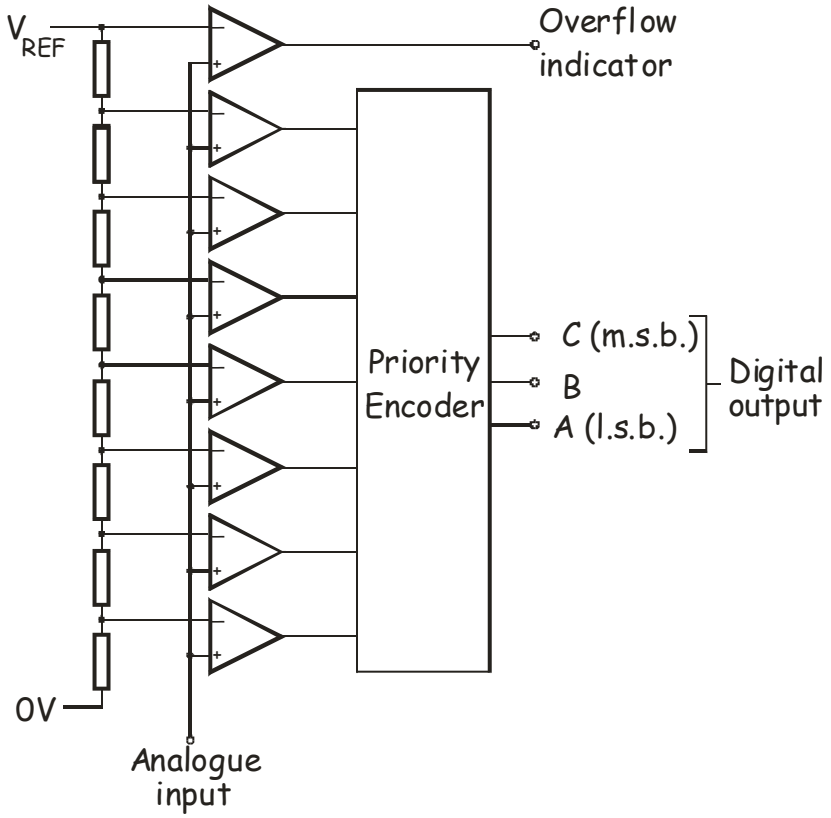


V_{OUT} = $+V_{SAT}$ when V_{IN} is smaller than V_{REF}.
V_{OUT} = $-V_{SAT}$ when V_{IN} is bigger than V_{REF}.
($+V_{SAT}$ = positive saturation voltage, $-V_{SAT}$ = negative saturation voltage.)

Now back to the task in hand, the flash converter.

3-bit Flash Converter

The basic circuit diagram for a 3-bit flash converter is shown below:



The design may vary in that the analogue input signal may be applied to the inverting input, instead of the non-inverting. In that case the reference voltages would be applied to the non-inverting inputs.

Notice that, in this case, the analogue input signal is connected directly to the inverting inputs of the eight comparators.

Their non-inverting inputs are connected to various points on a resistor chain. This chain creates a different reference voltage for each comparator. Each comparator compares the analogue input signal voltage with its reference voltage, and outputs a voltage at either positive or negative saturation level, following the rules outlined above. At this stage, the analogue signal has been converted into digital signals, but not into a pure binary number.

The outputs of the comparators become inputs for the priority encoder. This is a combinational logic system, like those studied in ET1. It converts the comparator outputs into a binary number.

The uppermost comparator in the system is used to indicate that the analogue signal has exceeded the voltage range that the ADC can handle. Usually, it does so by lighting an 'overflow' LED.

The main advantage of the flash converter is its speed. It takes very little time to convert the analogue signal into a binary number. The analogue signal is connected directly to each comparator. They simultaneously switch their outputs into either positive or negative saturation. (For this reason, this type of ADC is also known as a 'parallel A to D converter'.) The priority encoder consists of a number of logic gates, or equivalent, which, again rapidly, produces the required binary number output. This type of ADC is widely used in applications such as digitising video signals in TV tuner cards, where high conversion speed is essential.

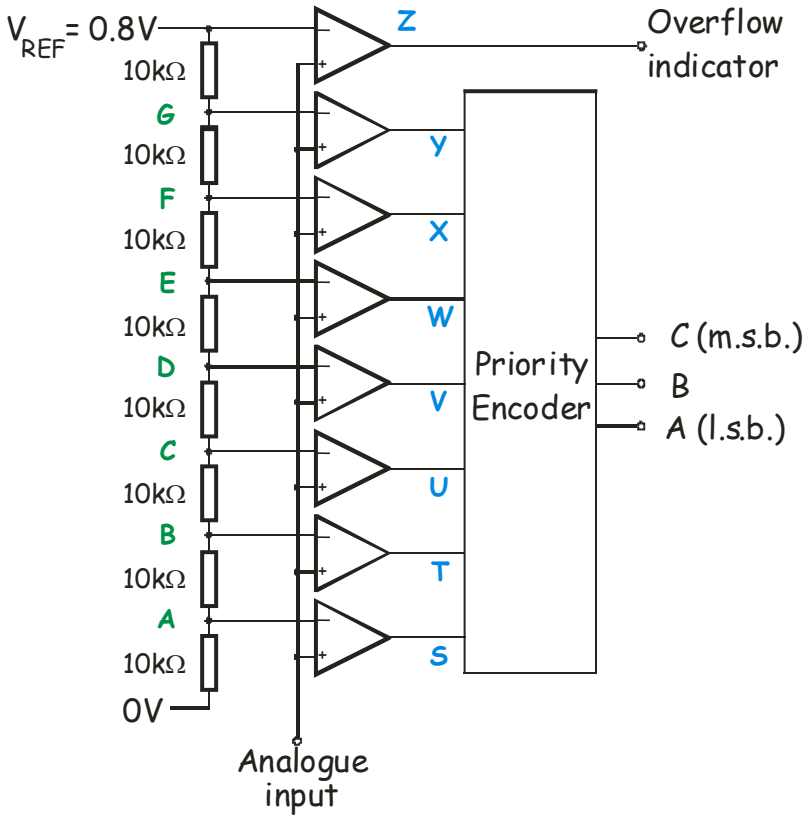
The main disadvantage is its cost. This is the result of the complexity of the circuit. Most digital systems manipulate data in the form of 8 bit binary numbers, or more. The circuit diagram shown earlier was for a 3-bit ADC. There are eight possible values for a three bit binary number – 000,001,010 etc. Each of these corresponds to a small range of analogue input voltages.

For example, if the 3-bit ADC is designed for analogue signals in the range 0 to 8V, then 000 would correspond to voltages from 0V to 1V, 001 from 1V to 2V, and so on. The circuit must be able to distinguish between these voltage ranges. To do so, there must be a comparator set up to respond to each of these ranges. This needs seven comparators, plus one more to detect the overflow condition.

In general, a n-bit ADC requires $2^n - 1$ comparators connected to the priority encoder, plus one for the overflow detection, making a total of 2^n comparators. For example, a 8-bit flash converter requires $2^8 = 256$ comparators. Hence it is an expensive circuit!

Analysing an ADC circuit:

Here is the same 3-bit ADC circuit diagram again, but this time with component values, reference voltage, and some labels, added.



The total resistance of the resistor chain R_T = 8 x 10kΩ = 80kΩ.
The voltage dropped across the chain V =0.8V.
We can ignore any current flowing into the inputs of the op-amps, as they have huge input impedance.
Hence the current flowing down the resistor chain is

$$I = V / R_T = 0.8/80 = 0.01mA.$$

This current flowing through a 10kΩ resistor creates a voltage drop across it of I x R = 0.01 x 10 = 0.1V, and so:

voltage at point **A** = 0.1V,
voltage at point **B** = 0.2V,
voltage at point **C** = 0.3V,
voltage at point **D** = 0.4V etc.

Assuming that the positive saturation voltage is +12V, and the negative saturation voltage is 0V, the behaviour of the comparators is described in the following table:

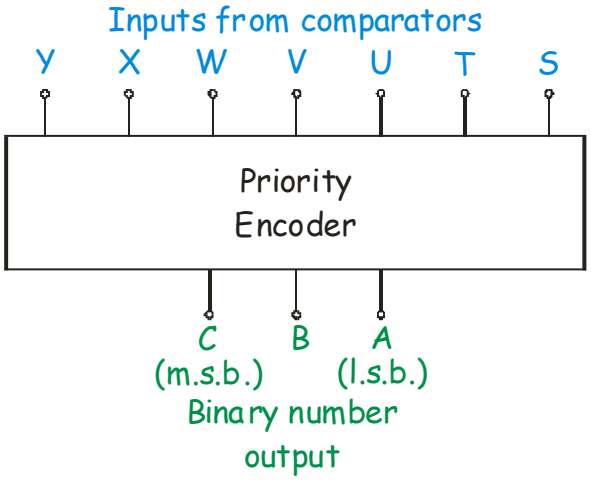
Analogue input V_{IN}	Comparator outputs / V						
	S	**T**	**U**	**V**	**W**	**X**	**Y**
V_{IN} < 0.1V	0	0	0	0	0	0	0
0.1V < V_{IN} < 0.2V	12	0	0	0	0	0	0
0.2V < V_{IN} < 0.3V	12	12	0	0	0	0	0
0.3V < V_{IN} < 0.4V	12	12	12	0	0	0	0
0.4V < V_{IN} < 0.5V	12	12	12	12	0	0	0
0.5V < V_{IN} < 0.6V	12	12	12	12	12	0	0
0.6V < V_{IN} < 0.7V	12	12	12	12	12	12	0
0.7V < V_{IN} < 0.8V	12	12	12	12	12	12	12
V_{IN} > 0.8V	**Z** =+12V indicating overflow						

The priority encoder:

The priority encoder is a combinational logic system. Its behaviour is specified in a truth table. For our purposes, assume that the system will see $+V_{SAT}$ (12V) as logic 1, and $-V_{SAT}$ (0V) as logic 0. For the 3-bit ADC shown earlier, the truth table then becomes:

Analogue input V_{IN}	Comparator outputs							Binary number output		
	S	T	U	V	W	X	Y	C	B	A
V_{IN} < 0.1V	0	0	0	0	0	0	0	0	0	0
0.1V < V_{IN} < 0.2V	1	0	0	0	0	0	0	0	0	1
0.2V < V_{IN} < 0.3V	1	1	0	0	0	0	0	0	1	0
0.3V < V_{IN} < 0.4V	1	1	1	0	0	0	0	0	1	1
0.4V < V_{IN} < 0.5V	1	1	1	1	0	0	0	1	0	0
0.5V < V_{IN} < 0.6V	1	1	1	1	1	0	0	1	0	1
0.6V < V_{IN} < 0.7V	1	1	1	1	1	1	0	1	1	0
0.7V < V_{IN} < 0.8V	1	1	1	1	1	1	1	1	1	1

Output, Z, of the overflow comparator takes no part in this discussion as it is not connected to the priority encoder. The 'Analogue input' column is retained to show the full picture, but again takes no part in the design.
The next diagram shows the inputs and outputs of the priority encoder logic system:



Converting the truth table into a combinational logic system is potentially a very complex problem. With seven inputs, there are theoretically 2^7 (= 128) possible input combinations. In reality, only the eight shown in the truth table can ever occur. The remaining 120 combinations can never occur and so are 'don't care' states, when it comes to generating Boolean expressions for the logic system.

For example, the analogue voltage V_{IN} cannot be greater than 0.3V (making **U** change to positive saturation,) without also being greater than 0.2V (turning **T** to positive saturation,) and being greater than 0.1V (turning **S** to positive saturation.) In other words, all lines of the truth table where **U** = 1 but **S** and **T** are logic 0 cannot exist.

By inspection, the following logic expressions are obtained:

$$C = V$$
$$B = S.T.\overline{V} + X$$
$$A = S.\overline{T} + U.\overline{V} + W.\overline{X} + Y$$

These could be generated using appropriate logic gates, or using a multiplexer or memory IC, as described in module ET1.

ADC Resolution:

This is a measure of the sensitivity of the ADC, i.e. how the output changes in response to changes in the input.

It is closely connected to two other parameters, the number of bits in the output, and the analogue input voltage range that the converter can handle.

We will now explore this connection.

Suppose we have a 3-bit ADC with an input voltage range of 4.0V.

There are eight possible outputs – 000, 001, 010, 011, 100, 101, 110 and 111. As the analogue input voltage changes, the converter will assign one of these eight numbers to it, in the following way:

- inputs less than 0.5V will cause the output number to be 000;
- inputs of 0.5V, or up to 1.0V will cause the output to be 001;
- inputs of 1.0V, or up to 1.5V will cause the output to be 010;

and so on until:

- inputs of 3.0V, or up to 3.5V will cause the output to be 110;
- inputs greater than 3.5V will cause the output to be 111;

If the input voltage exceeds 4.0V, the output will still be 111, but the overflow indicator will be activated.

Here the resolution is 0.5V. Whenever the input changes by more than 0.5V, there **must** be a change in the output number. A change of less than that may or may not cause the output to change. (If the input sits at 0.9V, and then increases by 0.2V, the output will change from 001 to 010. However, if the input sits at 1.2V and then increases by 0.2V, the output will not change.)

For a n-bit ADC, of the type shown in the circuit diagrams on pages 3 and 5, the resolution can be calculated using the formula:

$$\text{resolution} = \text{input voltage range} / 2^n$$

For example, given an 8-bit flash converter of this type with an input voltage range of 10V, then:

$$\text{resolution} = 10 / 2^8 = 10 / 256 = 0.0391\text{V}$$

Similarly, a flash converter with a 6-bit output and a resolution of 0.2V will have:

$$\begin{aligned}\text{input voltage range} &= \text{resolution} \times 2^n \\ &= 0.2 \times 26 \\ &= 12.8\text{V}\end{aligned}$$

Exercise 1 (Solutions will be given at the end of the topic.)

(a) A 2-bit flash converter has an input voltage range of 2.0V.
What is its resolution?

(b) What is the input voltage range of an 8-bit flash converter that has a resolution of 0.05V?

Designing a Flash ADC to meet a given specification:

The performance of the ADC can be described in a number of ways, including:

- the voltage range for the input;
- the number of bits that make up the output binary number;
- the resolution;
- the speed of conversion;
- the power supply used.

In this case we will design an ADC with the following parameters:

- number of output bits = 4;
- input voltage range = 0 to 4V;
- comparator outputs have positive saturation = +10V and negative saturation = 0V;

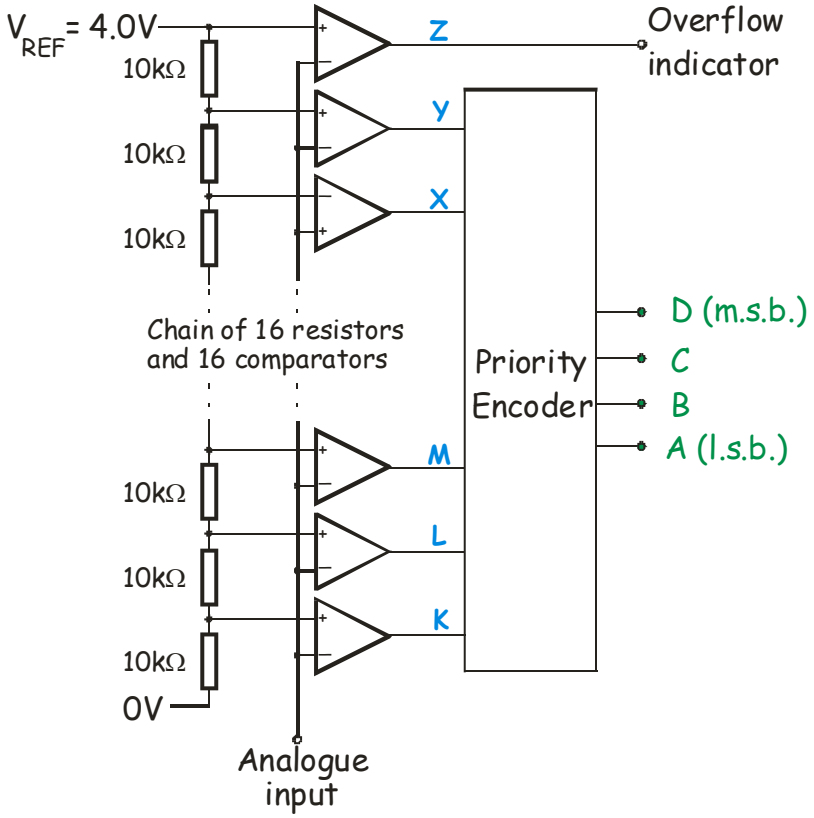
For a 4-bit flash converter we need sixteen ($=2^4$) comparators, and so sixteen equal sized resistors in the resistor chain to give a linear response (output number directly proportional to the input voltage.)

The input voltage range dictates the size of the reference voltage used.
In this case, the reference voltage will be 4V.

The resolution will be $4 / 2^4 = 0.25$V, using the formula given on page 9.

The sixteen resistors will carve up the 4V reference voltage into 0.25V chunks. The actual value of resistor used for the components of the chain is not important, provided that it is big enough to keep the current flowing down it, and so the power dissipation, to a manageably small size. The size should always be bigger than 1kΩ. In this case, we will use 10KΩ resistors.

Here is the circuit diagram for the ADC, though not drawn in full !
Purely to be different, the analogue input signal has been connected to the inverting inputs of the comparators this time.



The behaviour of the system is described in the table on the next page.

The priority encoder is designed in the same way as before, by examining the truth table. This time, we assume that a comparator output voltage of +10V is seen as logic 1, and an output of 0V is seen as logic 0 by the priority encoder.

Here are logic expressions for the priority encoder:

$$D = \overline{R}$$
$$C = \overline{M}.\overline{N}.R + \overline{V}$$
$$B = \overline{L}.N + \overline{P}.R + \overline{T}.V + \overline{X}$$
$$A = \overline{K}.L + \overline{M}.N + \overline{O}.P + \overline{Q}.R + \overline{S}.T + \overline{U}.V + \overline{W}.X + \overline{Y}$$

The overflow indicator functions as in the previous example.

	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	D	C	B	A
V_{IN} < 0.25V	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	0	0	0	0
0.25V < V_{IN} < 0.50V	0	10	10	10	10	10	10	10	10	10	10	10	10	10	10	0	0	0	1
0.50V < V_{IN} < 0.75V	0	0	10	10	10	10	10	10	10	10	10	10	10	10	10	0	0	1	0
0.75V < V_{IN} < 1.00V	0	0	0	10	10	10	10	10	10	10	10	10	10	10	10	0	0	1	1
1.00V < V_{IN} < 1.25V	0	0	0	0	10	10	10	10	10	10	10	10	10	10	10	0	1	0	0
1.25V < V_{IN} < 1.50V	0	0	0	0	0	10	10	10	10	10	10	10	10	10	10	0	1	0	1
1.50V < V_{IN} < 1.75V	0	0	0	0	0	0	10	10	10	10	10	10	10	10	10	0	1	1	0
1.75V < V_{IN} < 2.00V	0	0	0	0	0	0	0	10	10	10	10	10	10	10	10	0	1	1	1
2.00V < V_{IN} < 2.25V	0	0	0	0	0	0	0	0	10	10	10	10	10	10	10	1	0	0	0
2.25V < V_{IN} < 2.50V	0	0	0	0	0	0	0	0	0	10	10	10	10	10	10	1	0	0	1
2.50V < V_{IN} < 2.75V	0	0	0	0	0	0	0	0	0	0	10	10	10	10	10	1	0	1	0
2.75V < V_{IN} < 3.00V	0	0	0	0	0	0	0	0	0	0	0	10	10	10	10	1	0	1	1
3.00V < V_{IN} < 3.25V	0	0	0	0	0	0	0	0	0	0	0	0	10	10	10	1	1	0	0
3.25V < V_{IN} < 3.50V	0	0	0	0	0	0	0	0	0	0	0	0	0	10	10	1	1	0	1
3.50V < V_{IN} < 3.75V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	1	1	1	0
3.75V < V_{IN} < 4.00V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
V_{IN} > 4.00V	Z = 0V indicating overflow																		

Exercise 2 (Solutions will be given at the end of the topic.)

A less ambitious design task!
Design an ADC with the following parameters:

- number of output bits = 2;
- input voltage range = 0 to 3V;
- comparator outputs have positive saturation = +12V and negative saturation = 0V;

Your design should include:

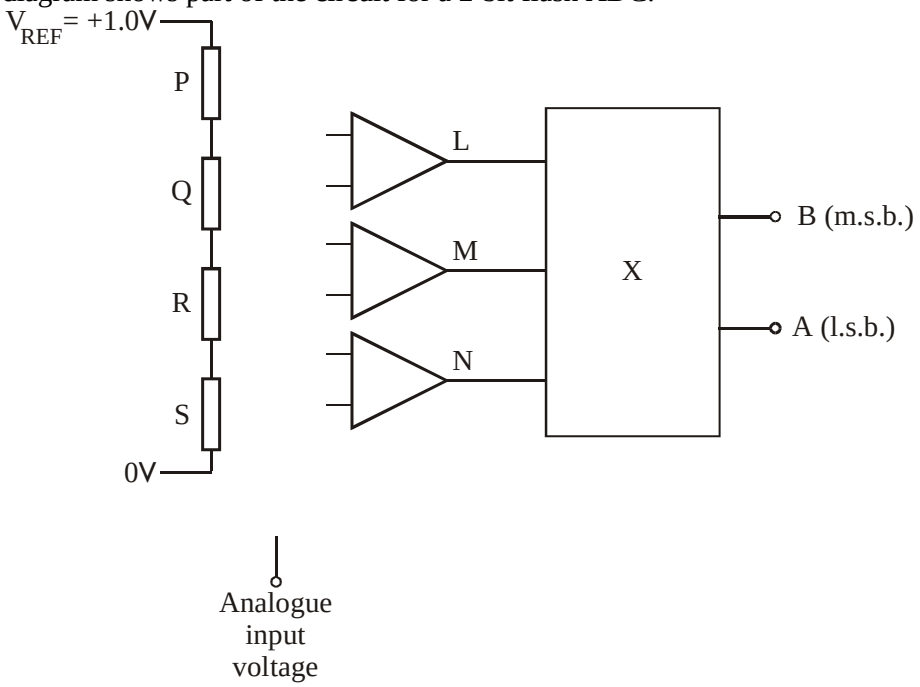
- a circuit diagram for the ADC with component values and reference voltage labelled;
- the resolution of the ADC;
- a table showing the operation of the circuit;
- Boolean expressions for the outputs of the priority encoder in terms of the inputs.

Module ET5
Electronic Systems Applications.

Practice Exam Questions:

1. A microprocessor systems can contain both an analogue-to-digital converter (ADC) and a digital-to-analogue converter (DAC)

(a) The diagram shows part of the circuit for a 2-bit flash ADC.



The system meets the following specification:

Analogue input voltage	Voltage at L	Voltage at M	Voltage at N	Binary output	
				B	A
0 to 0.25V	0V	0V	0V	0	0
0.25V to 0.50V	0V	0V	12V	0	1
0.50V to 0.75V	0V	12V	12V	1	0
0.75V to 1.00V	12V	12V	12V	1	1

(i) Complete the circuit diagram by:

- adding a fourth comparator so that its output indicates an overflow condition, when the analogue input voltage exceeds 1.0V;
- adding all connections needed;
- labelling the inverting inputs of the op-amps with a '-' and the non-inverting inputs with a '+'.

[4]

(ii) Calculate suitable values for resistors P, Q, R and S. [2]

……

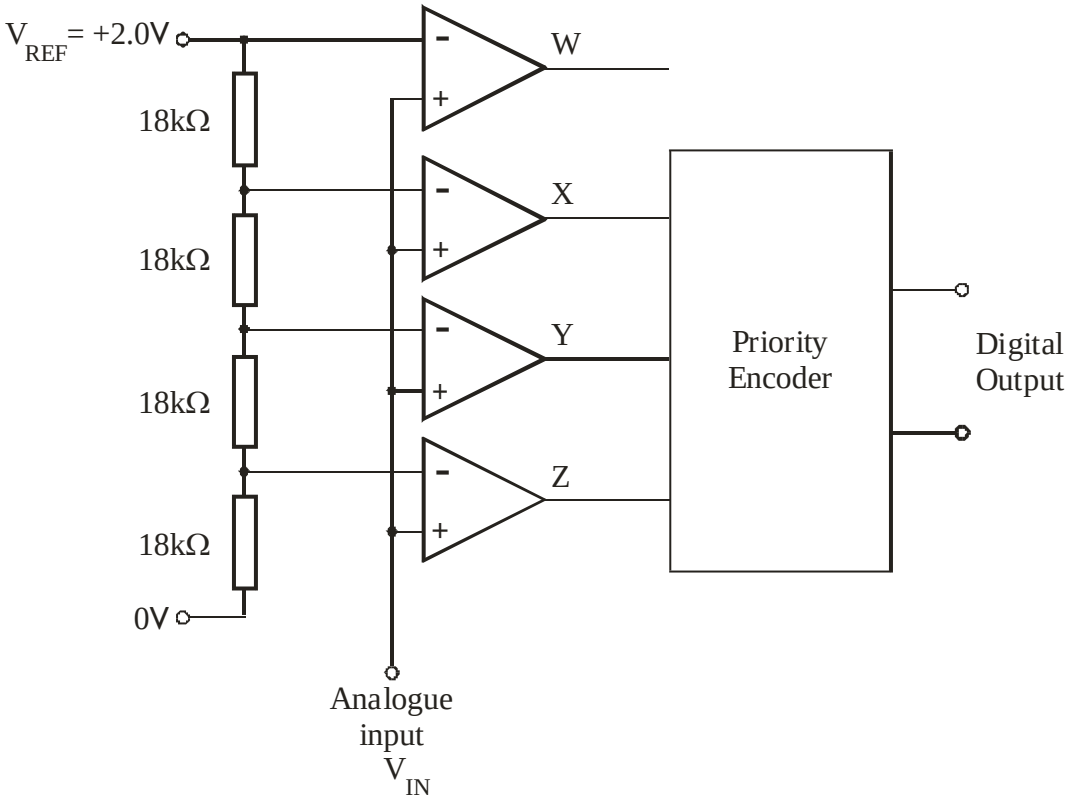
……

Resistor P = ... Resistor Q = ... Resistor R = ... Resistor S = ...

(iii) What is the name of the sub-system X, used to convert the output signals from the op-amps into a binary sequence. [1]

……

2. Here is the circuit diagram for an Analogue-to-Digital converter (ADC.)



(a) What is the name of this type of ADC? [1]

……..

(b) What is the function of the following components in this system: [2]

(i) Priority Encoder

……..

(ii) the comparator whose output is labelled W

……..

(c) Calculate the resolution of this ADC. [1]

……..

(d) What is the analogue input voltage range for this ADC [1]

……..

(e) V_{REF} is reduced to +1.0V. What is the effect of this change on:

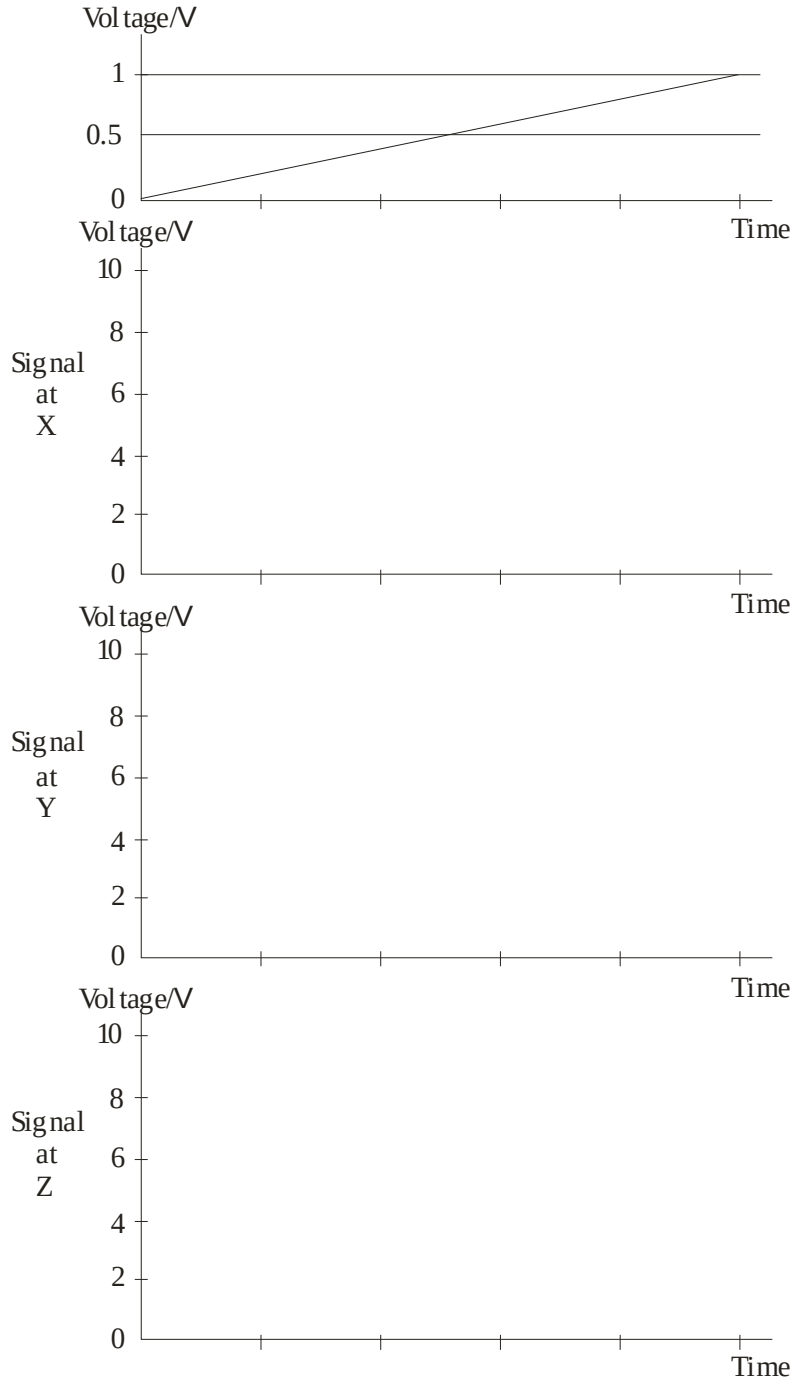
(i) resolution; [1]

……..

(ii) analogue input voltage range? [1]

……..

(f) The comparators have saturation voltages of +8V and +1V and V_{REF} is set at +1.0V.
The top graph shows how the input voltage V_{IN} changes over a period of time.
Use the axes provided to draw the signals at X, Y and Z over this time. [4]



Solutions to Exercises:

Exercise 1:

(a) Resolution = input voltage range / 2^n
= 2.0 / 2^2
= 0.5V

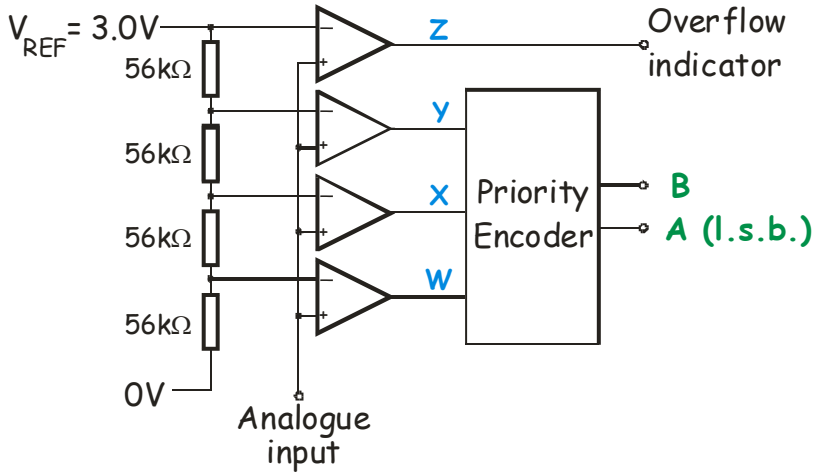
(b) Input voltage range = resolution x 2^n
= 0.05 x 2^8
= 12.8V

Exercise 2:

The 2-bit ADC has a resolution given by:

Resolution = input voltage range / 2^n
= 3 / 2^2
= 0.75V

The circuit requires $2^n = 2^2 = 4$ comparators and 4 equal sized resistors (all greater than 1kΩ). As the input voltage range = 0 to +3V, the reference voltage will be 3V. The circuit diagram is shown below:



(The resistor chain can have any value of resistor greater than 1kΩ, but all resistors must have the same value.)

The analogue input signal could be connected to the inverting inputs, with the reference voltages connected to the non-inverting inputs. In that case, all the voltages in the next table must be reversed – 12V → 0V, and 0V → 12V.)

The behaviour of the ADC is described in the following table:

Analogue input V_{IN}	Comparator outputs /V			Binary number at output	
	W	**X**	**Y**	**B**	***A***
V_{IN} < 0.75V	0	0	0	0	0
0.75V < V_{IN} < 1.50V	12	0	0	0	1
1.50V < V_{IN} < 2.25V	12	12	0	1	0
2.25V < V_{IN} < 3.00V	12	12	12	1	1
V_{IN} > 3.00V	**Z** =+12V indicating overflow				

The truth table for the priority encoder is:

Comparator outputs			Binary number at output	
W	**X**	**Y**	**B**	***A***
0	0	0	0	0
1	0	0	0	1
1	1	0	1	0
1	1	1	1	1

Boolean expressions for the priority encoder:

$$B = X$$
$$A = W.\overline{X} + Y$$